M. Tech. (VLSI) - 2021 Curriculum

Course Code	Semester – I	Credits
EC5101	Graph Theory and Optimization Techniques	4
EC5102	Basics of VLSI	3
EC5103	Semiconductor Device Modeling and Simulation	3
	Elective –I	3
	Elective –II	3
EC5104	Seminar	2
EC5105	HDL Programming Laboratory	2
EC5106	Device Modeling and Simulation Laboratory	2
	Total Credits	22

Course Code	Semester – II	Credits
EC5151	Analog IC Design	3
EC5152	VLSI System Testing	3
EC5153	ASIC Design	3
	Elective –III	3
	Elective –IV	3
EC5154	Comprehensive Viva-Voce	2
EC5155	Analog IC Design Laboratory	2
EC5156	ASIC – CAD Laboratory	2
	Total Credits	21

Course Code	Semester – III	Credits
EC6101	Project Work Phase – I	12
	Total Credits	12

Course Code	Semester – IV	Credits
EC6151	Project Work Phase – II	12
	Total Credits	12

Summary:

Branch	I Sem	II Sem	III Sem	IV Sem	Total
ECE	22	21	12	12	67

Electives:

Course Code	Electives	Credits
Semester I Electives		
EC5111	Advanced Digital System Design	3
EC5112	CAD for VLSI	3
EC5113	Optimizations of Digital Signal Processing Structures for VLSI	3
EC5114	VLSI Process Technology and Fabrication	3
EC5115	FPGA Based System Design	3
EC5116	Mixed-signal circuit design	3
EC5117	Embedded System Design	3
EC5118	Modelling and Synthesis with Verilog HDL / VHDL	3
EC5119	RF circuits	3
EC5120	DSP Architecture	3
Semester II Electives		
EC5121	Physics and Modeling of MOS Transistors	3
EC5122	Nano-Scale Devices: Modelling and Circuits	3
EC5123	CMOS Digital VLSI	3
EC5124	Physical Design Automation	3
EC5125	Asynchronous System Design	3
EC5126	Testability of Analog / Mixed-Signal Circuits and High-Speed Circuit Design	3
EC5127	VLSI Digital Signal Processing Systems	3
EC5128	Internet of Things	3
EC5129	Cognitive Radio	3
EC5130	Reliability of Devices and Circuits	3

FIRST SEMESTER

Course Code	:	**EC5101**
Course Title	:	**Graph Theory and optimization Techniques**
Number of Credits	:	**4-0-0-4**
Prerequisites (Course code)	:	**None**
Course Type	:	**Core**

Course outcomes: At the end of the course, the student will be able to:

CO1	Discuss the various types of graphs and their properties with examples.
CO2	Model given problems to analyse the underlying graph model.
CO3	Identify the planarity and non-planarity of graphs.
CO4	Apply matching theory to solve problems.
CO5	Perform graph traversals and find shortest path.

Course Content:

Basic definitions, examples and some results, relating degree, walk, trail, path, tour, cycle, complement of a graph, self-complementary graph, Connectedness, Connectivity, distance, shortest path, radius, diameter and Bipartite graphs. Some eccentric properties of graphs, tree, spanning tree, coding of spanning tree. Number of spanning trees in a complete graph. Recursive procedure to find number of spanning trees. Construction of spanning trees

Directed graphs: some standard definitions and examples of strongly, weakly, unilaterally connected digraphs, strong components and deadlock. Matrix representation of graph and digraphs. Some properties (proof not expected). Eulerian graphs and standard results relating to characterization of Eulerian graphs. Hamiltonian graph-standard theorems (Dirac theorem, Chavtal theorem, closure of graph). Non-Hamiltonian graph with maximum number of edges. Self-centered graphs and related simple theorems.

Chromatic number; vertex chromatic number of a graph, edge chromatic number of a graph (only properties and examples)-application to colouring. Planar graphs, Euler's formula, maximum number of edges in a planar graph, some problems related to planarity and non-planarity, Five colour theorem, Vertex Covering, Edge Covering, Vertex independence number, Edge independence number, relation between them and number of vertices of a graph.

Matching theory, maximal matching and algorithms for maximal matching. Perfect matching (only properties and applications to regular graphs). Tournaments, some simple properties and theorems on strongly connected tournaments. Application of Eulerian digraphs

DFS-BFS algorithm, shortest path algorithm, Min-spanning tree and Max-spanning tree algorithm, Planarity algorithm. Flows in graphs; Maxflow mincut theorem, algorithm for maxflow. PERT-CPM. Complexity of algorithms; P-NP-NPC-NP hard problems and examples.

Text Books:

1. J.A.Bondy and U.S.R.Murthy, “Graph Theory with Applications”, Macmillan, London, 1976, EBook, Freely Downloadable.
2. Cormen, Leiserson, Rivest and Stein, “Introduction to Algorithms”, 2nd Edition, McGraw-Hill, 2001.

Reference Books:

1. M.Gondran and M.Minoux,“Graphs and Algorithms”, John Wiley, 1984.
2. H.Gerez, “Algorithms for VLSI Design Automation”, John Wiley, 1999.

Course Code	:	**EC5102**
Course Title	:	**Basics of VLSI**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Core**

Course outcomes: At the end of the course, the student will be able to:

CO1	Implement the logic circuits using MOS and CMOS technology.
CO2	Analyze various circuit configurations and their applications.
CO3	Evaluate the merits of circuits according to the technology and applications.
CO4	Design low power CMOS VLSI circuits.
CO5	Examine the rapid advances in CMOS Technology.

Course Content:

Introduction to CMOS circuits: MOS transistors, CMOS combinational logic gates, multiplexers, latches and flip-flops, CMOS fabrication and layout, VLSI design flow

MOS transistor theory: Ideal I-V and C-V characteristics, non-ideal I-V effects, DC transfer characteristics, Switch level RC delay models.

CMOS technologies: Layout design rules, CMOS process enhancement, Technology related CAD issues

Circuit characterization and performance estimation: Delay estimation, Logical effort and transistor sizing, Power dissipation, Interconnect design margin, Reliability, Scaling.

Combinational circuit design: Static CMOS, Ratioed circuits, Cascode voltage switch logic, Dynamic circuits, Pass transistor circuits.

Text Books:

1. N.H.E.Weste and D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Pearson, 2011.
2. J.Rabey and B. Nikolic, "Digital Integrated circuits", 2nd Edition, Pearson, 2003.

Reference Books:

1. Pucknell and Eshraghian, "Basic VLSI Design", 3rd Edition, PHI, 1996.
2. Recent literature in Basics of VLSI.

Course Code	:	**EC5103**
Course Title	:	**Semiconductor Device Modelling and Simulation**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Core**

Course outcomes: At the end of the course, the student will be able to:

CO1	Illustrate the importance of four major building blocks of semiconductor devices.
CO2	Discuss the physics behind the semiconductor device model and the parameters.
CO3	Explain the terminal behaviour and compact models of most microelectronic semiconductor devices.
CO4	Inspect the suitability of a semi-conductor device for a given circuit application.
CO5	Design the basic semiconductor devices to meet specific figures of merit.

Course Content:

Concentration and motion of carriers in Semiconductor bulk - equilibrium concentration in intrinsic and extrinsic semiconductors, excess carriers, drift and diffusion transport, continuity equation. Concentration and motion of carriers at the interface - surface recombination, surface mobility.

Device modeling - basic equations for device analysis, approximation to these equations for deriving analytical expressions. PN homo-junction - ideal static I-V characteristics and deviations including breakdown, ac small signal equivalent circuit, switching characteristics.

BJT - transistor action, static characteristics, ac small signal equivalent circuit, switching characteristics, compact models.

MIS Junction/capacitor - ideal C-V characteristics and deviations due to interface states/charges and work function differences, threshold voltage.

FETs - field effect, types of transistors (JFET, MESFET, MISFET), static characteristics of MISFET, small signal equivalent circuit, difference between BJT and FET compact models.

Text Books:

1. Streetman, Ben G., and Sanjay Banerjee, "Solid state electronic devices", Prentice-Hall of India, 2001.
2. S. M. Sze, "Physics of Semiconductor Devices", 2nd edition, Wiley Eastern, 1981.

Reference Books:

1. Sah, Chih-Tang, "Fundamentals of solid-state electronics", World Scientific, 1991.
2. Tyagi, Man S, "Introduction to semiconductor materials and devices", John Wiley and Sons, 2008.

Course Code	:	**EC5105**
Course Title	:	**HDL Programming Laboratory**
Number of Credits	:	**0-0-3-2**
Prerequisites (Course code)	:	**EC5102**
Course Type	:	**ELR**

Course outcomes: At the end of the course, the student will be able to:

CO1	Simulate adders, multiplexers, code converters for the given specifications.
CO2	Evaluate the performance for the design parameters.
CO3	Design and test memory elements.
CO4	Use pipelining for efficient multiplier designs.
CO5	Apply pipelining for efficient FIR filter designs

Course Content:

1. Adder/ Subtractor
2. Multiplexer/ Demultiplexer
3. Encoder/ Priority Encoder
4. Code Converter
5. Flipflop
6. Shift Register/ Universal Shift Register
7. Comparator
8. Upcounter/ Downcounter
9. Udps
10. Memory – ROM, RAM
11. Array Multiplier/ Array Multiplier With Pipelining
12. Fir Filter/ Fir Filter With Pipelinig

Course Code	:	**EC5106**
Course Title	:	**Device Modeling and Simulation Laboratory**
Number of Credits	:	**0-0-3-2**
Prerequisites (Course code)	:	**EC5103**
Course Type	:	**ELR**

Course outcomes: At the end of the course, the student will be able to:

CO1	Use Verilog –A for simulations.
CO2	Model and extract the diode parameters for the specific design.
CO3	Implement compact Transistor models using Verilog –A.
CO4	Design amplifiers through simulations for the given specifications.
CO5	Characterize and verify the semiconductor devices.

Course Content:

1. Introduction to SPICE simulations using Verilog-A
2. Compact modeling and parameter extraction of diode
3. DC and AC simulations of diode circuits using Verilog-A model in SPICE
4. Characterization of BJTs and MOSFETs using TCAD/SPICE
5. Parameter extraction for BJT and MOSFET compact models
6. Implementing BJT compact model using Verilog-A
7. Implementing MOSFET compact model in SPICE
8. Characterization of self-heating in semiconductor devices
9. Building amplifiers using MOSFET and BJT models using SPICE
10. TCAD simulation process of semiconductor devices

SECOND SEMESTER

Course Code	:	**EC5151**
Course Title	:	**Analog IC Design**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Core**

Course outcomes: At the end of the course, the student will be able to:

CO1	Devise equivalent circuits of MOS based Analog VLSI to analyze their performance.
CO2	Design analog VLSI circuits for the given specification.
CO3	Analyse the frequency response of different configurations of an amplifier.
CO4	Review the feedback topologies involved in amplifier design.
CO5	Evaluate the design features of differential amplifiers.

Course Content:

Basic MOS Device Physics – General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.

Differential Amplifiers – Single Ended and Differential Operation, Basic Differential Pair, Common Mode Response, Differential Pair with MOS loads, Gilbert Cell. Passive and Active Current Mirrors – Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors

Frequency Response of Amplifiers – General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.

Feedback Amplifiers – General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps. Stability and Frequency Compensation

Bandgap References, Introduction to Switched Capacitor Circuits, Nonlinearity and Mismatch

Text Books:

1. B.Razavi, “Design of Analog CMOS Integrated Circuits”, 2nd Edition, McGraw Hill Edition, 2016.
2. Paul. R.Gray and Robert G. Meyer, “Analysis and Design of Analog Integrated Circuits”, Wiley, 5th Edition, 2009.
3. T. C. Carusone, D. A. Johns and K. Martin, “Analog Integrated Circuit Design”, 2nd Edition, Wiley, 2012.

Reference Books:

1. P.E.Allen and D.R. Holberg, "CMOS Analog Circuit Design", 3rd Edition, Oxford University Press, 2011.
2. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rd Edition, Wiley, 2010.

Course Code	:	**EC5152**
Course Title	:	**VLSI System Testing**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Core**

Course outcomes: At the end of the course, the student will be able to:

CO1	Apply the concepts of testing to obtain better results in IC design.
CO2	Solve the problems associated with testing of semiconductor circuits at earlier design levels.
CO3	Analyse the various test generation methods for static and dynamic CMOS circuits.
CO4	Identify the methods to test combinational and sequential CMOS circuits.
CO5	Recognize BIST techniques for improving testability.

Course Content:

Basics of Testing: Fault models, Combinational logic and fault simulation, Test generation for Combinational Circuits. Current sensing based testing. Classification of sequential ATPG methods. Fault collapsing and simulation

Universal test sets: Pseudo-exhaustive and iterative logic array testing. Clocking schemes for delay fault testing. Testability classifications for path delay faults. Test generation and fault simulation for path and gate delay faults.

CMOS testing: Testing of static and dynamic circuits. Fault diagnosis: Fault models for diagnosis, Cause-effect diagnosis, Effect-cause diagnosis.

Design for testability: Scan design, Partial scan, use of scan chains, boundary scan, DFT for other test objectives, Memory Testing.

Built-in self-test: Pattern Generators, Estimation of test length, Test points to improve testability, Analysis of aliasing in linear compression, BIST methodologies, BIST for delay fault testing.

Text Books:

1. N. Jha and S.D. Gupta, “Testing of Digital Systems”, Cambridge, 2003.
2. W. W. Wen, “VLSI Test Principles and Architectures Design for Testability”, Morgan Kaufmann Publishers. 2006.
3. Michael L. Bushnell and Vishwani D. Agrawal,” Essentials of Electronic Testing for Digital, memory and Mixed signal VLSI Circuits”, Kluwar Academic Publishers. 2000.

Reference Books:

1. P. K. Lala,” Digital circuit Testing and Testability”, Academic Press. 1997.
2. M. Abramovici, M. A. Breuer, and A.D. Friedman, “Digital System Testing and Testable Design”, Computer Science Press, 1990.
3. Recent literature in VLSI System Testing.

Course Code	:	**EC5153**
Course Title	:	**ASIC Design**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Core**

Course outcomes: At the end of the course, the student will be able to:

CO1	Demonstrate VLSI tool-flow and develop FPGA and CPLD architectures.
CO2	Analyze the issues involved in ASIC design, including technology choice, design management and tool-flow.
CO3	Construct ASIC algorithms.
CO4	Illustrate Full Custom Design Flow and the tools used.
CO5	Examine Semicustom Design Flow and the tools used - from RTL to GDS and Logical to Physical Implementation.

Course Content:

Introduction to Technology, Types of ASICs, VLSI Design flow, Design and Layout Rules, Programmable ASICs - Antifuse, SRAM, EPROM, EEPROM based ASICs. Programmable ASIC logic cells and I/O cells. Programmable interconnects. Advanced FPGAs and CPLDs and Soft-core processors

ASIC physical design issues, System Partitioning, Floorplanning and Placement. Algorithms: K-L, FM, Simulated annealing algorithms. Full Custom Design: Basics, Needs and Applications. Schematic and layout basics, Full Custom Design Flow.

Semicustom Approach: Synthesis (RTL to GATE netlist) - Introduction to Constraints (SDC), Introduction to Static Timing Analysis (STA). Place and Route (Logical to Physical Implementation): Floorplan and Power-Plan, Placement, Clock Tree Synthesis (clock planning), Routing, Timing Optimization, GDS generation

Extraction, Logical equivalence and STA: Parasitic Extraction Flow, STA: Timing Flow, LEC: Introduction, flow and Tools used. Physical Verification: Introduction, DRC, LVS and basics of DFM

System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. High performance algorithms for ASICs/ SoCs as case studies – Canonic Signed Digit Arithmetic, KCM, Distributed Arithmetic, High performance digital filters for sigma-delta ADC.

Text Books:

1. M.J.S. Smith, “Application Specific Integrated Circuits”, Pearson, 2003.
2. SudeepPasrichaandNikilDutt, “On-Chip Communication Architectures System on Chip Interconnect”, Elsevier, 2008.
3. H.Gerez, “Algorithms for VLSI Design Automation”, John Wiley, 1999.

Reference Books:

1. Jan.M.Rabaey et al, “Digital Integrated Circuit Design Perspective”, 2nd Edition, PHI 2003
2. David A.Hodges, “Analysis and Design of Digital Integrated Circuits”, 3rd Edition, MGH 2004.
3. Hoi-Jun Yoo, Kangmin Lee and Jun Kyong Kim, “Low-Power NoC for High-Performance SoC Design”, CRC Press, 2008.

Course Code	:	**EC5155**
Course Title	:	**Analog IC Design Laboratory**
Number of Credits	:	**0-0-3-2**
Prerequisites (Course code)	:	**EC5151**
Course Type	:	**ELR**

Course outcomes: At the end of the course, the student will be able to:

CO1	Characterize the MOS transistors.
CO2	Design FET Amplifier for the given load.
CO3	Implement and Test current mirrors.
CO4	Implement and Test Cascode Amplifiers.
CO5	Devise and Test Two stage Operational Amplifier.

Course Content:

1. Characteristics of NMOS and PMOS Transistor
2. Design of Common Source Amplifier with different Loads
3. Design of Common Gate Amplifier
4. Design of Common Drain Amplifier
5. Design of Single stage Cascode Amplifiers
6. Design of Current Mirrors
7. Design of Differential Amplifiers with Different Loads
8. Design of Two stage Opamp
9. Design of Telescopic Cascode Opamp
10. Design of Folded Cascode Opamp

Course Code	:	**EC5156**
Course Title	:	**ASIC – CAD Laboratory**
Number of Credits	:	**0-0-3-2**
Prerequisites (Course code)	:	**EC5152**
Course Type	:	**ELR**

Course outcomes: At the end of the course, the student will be able to:

CO1	Simulate Adders, Subtractors for the given specifications.
CO2	Design Multiplexers and Counters for the given specifications.
CO3	Design Accumulator for the given specifications.
CO4	Devise and Test Memory for the given specifications.
CO5	Compare the design methodologies with CAD software from different vendors.

Course Content:

1. Adder/ Subtractor
2. Multiplexer/ Demultiplexer
3. 8-bit Counter
4. Signed Pipelined Multiplier
5. Accumulator
6. MAC
7. Memory

The above experiments are carried out using the following tools:

1. Model SIM
2. Cadence
3. Synopsis
4. Mentor Graphics
5. Xilinx Plan ahead

ELECTIVES

Course Code	:	**EC5111**
Course Title	:	**Advanced Digital System Design**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Identify mapping algorithms into architectures.
CO2	Summarize various delays in combinational circuit and its optimization methods.
CO3	Design circuits with latches and flip-flops.
CO4	Construct combinational and sequential circuits based on VLSIs, and programmable logic devices.
CO5	Examine the advanced reconfigurable computing methods.

Course Content:

Mapping algorithms into Architectures: Data path synthesis, control structures, critical path and worst case timing analysis. FSM and Hazards.

Combinational network delay. Power and energy optimization in combinational logic circuit. Sequential machine design styles. Rules for clocking. Performance analysis.

Sequencing static circuits. Circuit design of latches and flip-flops. Static sequencing element methodology. Sequencing dynamic circuits. Synchronizers.

Data path and array subsystems: Addition / Subtraction, Comparators, counters, coding, multiplication and division. SRAM, DRAM, ROM, serial access memory, context addressable memory.

Reconfigurable Computing- Fine grain and Coarse grain architectures, Configuration architecturesSingle context, Multi context, partially reconfigurable, Pipeline reconfigurable, Block Configurable, Parallel processing.

Text Books:

1. N.H.E.Weste, and D. Harris, "CMOS VLSI Design", 4th edition, Pearson, 2010.
2. W.Wolf, "FPGA- based System Design", Pearson, 2004.
3. S.Hauck and A.DeHon, "Reconfigurable computing: the theory and practice of FPGA-based computation", Elsevier, 2008

Reference Books:

1. F.P. Prosser and D. E. Winkel, "Art of Digital Design", 1987
2. R.F.Tinde, "Engineering Digital Design", 2nd edition, Academic Press, 2000.
3. C. Bobda, "Introduction to reconfigurable computing", Springer, 2007.

Course Code	:	**EC5112**
Course Title	:	**CAD for VLSI**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Describe layout techniques in IC.
CO2	Identify algorithms required for circuit simulators.
CO3	Perform timing analysis and floor planning.
CO4	Apply scripting language PERL to improve EDA tool flow
CO5	Explain compaction techniques in IC.

Course Content:

Introduction to Design Methodologies: The VLSI Design Problem, Design Methods and Technologies, Layout Methodologies, Top-Down Approach: Routing: Fundamentals, Global Routing, Detailed Routing.

Performance Issues in Circuit Layout: Delay Models, Timing Driven Placement, Timing Driven Routing, Power Minimization.

Single-Layer Routing and Applications: Planar Subset Problem, Single-Layer Global Routing, Over-the-cell Routing, Multichip Modules, Wire-Length and Bend Minimization Techniques.

Cell Generation and Programmable Structures: Programmable Logic Arrays, Transistor Chaining, Weinberger Arrays and Gate Matrix Layout, CMOS Cell Layout Styles Considering Performance Issues.

Compaction: 1D Compaction, 2D Compaction

Text Books:

1. S.H. Gerez, Algorithms for VLSI Design Automation, Wiley, 2006.
2. M. Sarrafzadeh and C. K. Wong, An Introduction to VLSI Physical Design, McGraw Hill, 1996

Reference Books:

1. N.A.Sherwani, “Algorithms for VLSI Physical Design Automation”, Kluwer, 2012.
2. S.M. Sait, H. Youssef, “VLSI Physical Design Automation”, Cambridge India, 2010

Course Code	:	**EC5113**
Course Title	:	**Optimizations of Digital Signal Processing Structures for VLSI**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Summarize DSP concepts and design architectures.
CO2	Analyze the performance of DSP system through various transformation and optimization techniques.
CO3	Perform pipelining and parallel processing on FIR and IIR systems.
CO4	Characterize design in terms of computation complexity and speed.
CO5	Identify clock based issues and design asynchronous and wave pipelined systems.

Course Content:

An overview of DSP concepts, Pipelining of FIR filters. Parallel processing of FIR filters. Pipelining and parallel processing for low power, Combining Pipelining and Parallel Processing.

Transformation Techniques: Iteration bound, Retiming, Folding and Unfolding

Pipeline interleaving in digital filters. Pipelining and parallel processing for IIR filters. Low power IIR filter design using pipelining and parallel processing, Pipelined adaptive digital filters.

Algorithms for fast convolution: Cook-Toom Algorithm, Cyclic Convolution. Algorithmic strength reduction in filters and transforms: Parallel FIR Filters, DCT and inverse DCT, Parallel Architectures for Rank-Order Filters.

Synchronous pipelining and clocking styles, clock skew and clock distribution in bit level pipelined VLSI designs. Wave pipelining, constraint space diagram and degree of wave pipelining, Implementation of wave-pipelined systems, Asynchronous pipelining.

Text Books:

1. K.K.Parhi, "VLSI Digital Signal Processing Systems: Design And Implementation", JohnWiley, 2010.
2. Wayne Burleson, Konstantinos Konstantinides, Teresa H. Meng, "VLSI Signal Processing", 1996.

Reference Books:

1. U. Meyer -Baese, "Digital Signal Processing with FPGAs", Springer, 2014.
2. Richard J. Higgins, "Digital signal processing in VLSI", 1990.

Course Code	:	**EC5114**
Course Title	:	**VLSI Process Technology and Fabrication**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Describe the various techniques involved in the VLSI fabrication process.
CO2	Compare the different lithography methods and etching process.
CO3	Explain the deposition and diffusion mechanisms.
CO4	Analyse the fabrication of NMOS, CMOS memory and bipolar devices.
CO5	Evaluate the nuances in assembly and packaging of VLSI devices.

Course Content:
Electron grade silicon. Crystal growth. Wafer preparation. Vapour phase and molecular beam epitaxy. SOI. Epitaxial evaluation. Oxidation techniques, systems and properties. Oxidation defects.

Optical, electron, X-ray and ion lithography methods. Plasma properties, size, control, etch mechanism, etch techniques and equipments.

Deposition process and methods. Diffusion in solids. Diffusion equation and diffusion mechanisms.

Ion implantation and metallization. Process simulation of ion implementation, diffusion, oxidation, epitaxy, lithography, etching and deposition. NMOS, CMOS, MOS memory and bipolar IC technologies. IC fabrication

Analytical and assembly techniques. Packaging of VLSI devices

Text Books:

1. S.M.Sze, "VLSI Technology, 2nd edition , McGraw Hill, 1988.
2. W. Wolf, "Modern VLSI Design", 3rd edition, Pearson, 2002.

Reference Books:

1. James D. Plummer, "Silicon VLSI Technology: Fundamentals, Practice and Modeling", Pearson Education, 2000.
2. Stephen A. Campbell, "The Science and Engineering of Microelectronic Fabrication", 2nd edition, Oxford University Press 2001.

Course Code	:	**EC5115**
Course Title	:	**FPGA Based System Design**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Examine FPGA design flow.
CO2	Identify the building blocks of commercially available FPGA/CPLDs.
CO3	Develop VHDL/Verilog models and synthesize targeting for Vertex, Spartan FPGAs.
CO4	Devise parameterized library cells and implement system designs.
CO5	Summarize the routing terminologies and approaches used in FPGA architectures.

Course Content:

INTRODUCTION TO FPGAs: Evolution of programmable devices, FPGA Design flow, Applications of FPGA

DEISGN EXAMPLES USING PLDs: Design of Universal block, Memory, Floating point multiplier, Barrel shifter

FPGAs/CPLDs: Programming Technologies, Commercially available FPGAs, Xilinx's Vertex and Spartan, Actel's FPGA, Altera's FPGA/CPLD.

Building blocks of FPGAs/CPLDs: Configurable Logic block functionality, Routing structures, Input/output Block, Impact of logic block functionality on FPGA performance, Model for measuring delay. Q

Routing Architectures: Routing terminology, general strategy for routing in FPGAs, routing for row – based FPGAs, introduction to segmented channel routing, routing for symmetrical FPGAs, example of routing in a symmetrical FPGA, general approach to routing in symmetrical FPGAs, independence from FPGA routing architectures, FPGA routing structures. FPGA architectural assumptions, the logic block, the connection block, connection block topology, the switch block, switch block topology, architectural assumptions for the FPGA

CASE STUDY – Applications using Kintex-7, Viretex-7, Artix-7.

Text Books:

1. John V. Old Field, and Richrad C. Dorf, "Field Programmable Gate Arrays", Wiley, 2008.
2. Data sheets of Artix-7, Kintex-7, Virtex-7

Reference Books:

1. Stephen D. Brown, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic, "Field Programmable Gate Arrays", 2nd Edition, Springer, 1992.

Course Code	:	**EC5116**
Course Title	:	**Mixed-signal circuit design**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Describe the fundamentals of data converters and evaluate their performances.
CO2	Develop the methodology to design mixed signal IC using gm/Id concept.
CO3	Analyse the design of current mirrors and operational amplifiers
CO4	Experiment CMOS digital circuits and their implementation.
CO5	Design the frequency and Q tunable time domain filters.

Course Content:
Concepts of Mixed-Signal Design and Performance Measures. Introduction and Principle behind ADC's and DAC's - Performance Metrics of ADCs and DACs, Nyquist Rate DACs, Comparators Characterization – Two stage comparators – open loop comparators, Nyquist rate ADCs: Flash, SAR, Pipelined, Time-interleaved ADCs. Overview of oversampling ADCs

Design methodology for mixed signal IC design using gm/Id concept.

Design of Current mirrors. References. Comparators and Operational Amplifiers.

CMOS Digital Circuits Design: Design of MOSFET Switches and Switched-Capacitor Circuits, Layout Considerations.

Design of frequency and Q tunable continuous time filters.

Text Books:

1. David A. Johns and Ken Martin, "Analog Integrated Circuit Design", John Wiley and Sons, 1997.
2. B. Razavi, "Principles of Data Conversion System Design", Wiley-IEEE Press.

Reference Books:

1. R. J. Baker, Wiley, "CMOS Mixed Signal Circuit Design".
2. M.Gustavsson, J. J. Wikner, and N. N. Tan, Kluwer, "CMOS Data Conversion for Communications".

Course Code	:	**EC5117**
Course Title	:	**Embedded System Design**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Compare embedded system with general purpose system.
CO2	Describe the methods adapted for the development of a typical embedded system.
CO3	Explain RTOS and related mechanisms.
CO4	Discuss the kernel features, context switching, scheduling and time, memory managements.
CO5	Assess embedded system development environment and hardware testing methods.

Course Content:

Introduction to Embedded system, embedded system examples, Parts of Embedded System Typical Processor architecture, Power supply, clock, Cache memory, memory interface, interrupt, I/O ports, Buffers, Programmable Devices, ASIC etc. Bus architecture -I 2C, SPI, AMBA, CAN. Memory Technologies – EPROM, Flash, OTP, SRAM, DRAM, SDRAM etc

Introduction to Cypress Programmable System on Chip (PSoC). Structure of PSoC, PSoC Designer, PSoC Modules, Interconnects, Memory Management, Global Resources, Design Examples

Embedded System product Development Life cycle (EDLC), Specifications, Component selection, Schematic Design, PCB layout, fabrication and assembly. Product enclosure Design and Development. Concept of firmware, operating system and application programs. Power supply Design. External Interfaces.

Basic Features of an Operating System, Kernel Features [polled loop system, interrupt driven system, multi rate system], Processes and Threads, Context Switching, Scheduling[RMA, EDF, fault tolerant scheduling], Inter-process Communication, real Time memory management [process stack management, dynamic allocation], I/O [synchronous and asynchronous I/O, Interrupts Handling, Device drivers], RTOS [VxWorks, RT-LINUX].

Embedded System Development Environment – IDE, Cross compilation, Simulators/Emulators, Hardware Debugging. Hardware testing methods like Boundary Scan, In Circuit Testing (ICT) etc.

Text Books:

1. Shibu, "K.V. Introduction to Embedded Systems" Tata McGraw Hill, 2009.
2. Marilyn Wolf, "Computers as components: Principles of Embedded Computing System Design" Elsevier, 2012.
3. Raj Kamal, "Embedded systems Architecture, Programming and Design", Second Edition, 2008.

Reference Books:

1. Lyla B Das, "Embedded Systems: An Integrated Approach", Pearson, 2013.

2. Robert Ashby Designer's Guide to the Cypress PSoCNewnes (An imprint of Elsevier), 2006.
3. Oliver H. Bailey the Beginner's Guide to PSoC Express Timelines Industries Inc.

Course Code	:	**EC5118**
Course Title	:	**Modelling and Synthesis with Verilog HDL / VHDL**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Summarize the basic concepts of Verilog HDL.
CO2	Model digital systems in Verilog HDL at different levels of abstraction.
CO3	Implement the simulation techniques and test bench creation.
CO4	Distinguish the design flow of simulation from synthesizable version.
CO5	Examine the process of synthesis and post-synthesis.

Course Content:

Hardware modeling with the Verilog HDL. Encapsulation, modeling primitives, different types of description

Logic system, data types and operators for modeling in Verilog HDL. Verilog Models of propagation delay and net delay path delays and simulation, inertial delay effects and pulse rejection

Behavioral descriptions in Verilog HDL. Synthesis of combinational logic.

HDL-based synthesis - technology-independent design, styles for synthesis of combinational and sequential logic, synthesis of finite state machines, synthesis of gated clocks, design partitions and hierarchical structures.

Synthesis of language constructs, nets, register variables, expressions and operators, assignments, and compiler directives. Switch-level models in Verilog. Design examples in Verilog.

Text Books:

1. M.D.Ciletti, “Modeling, Synthesis and Rapid Prototyping with the Verilog HDL”, PHI, 1999.
2. S. Palnitkar, “Verilog HDL – A Guide to Digital Design and Synthesis”, Pearson, 2003.

Reference Books:

1. J Bhaskar, “A Verilog HDL Primer (3rd edition)”, Kluwer, 2005
2. M.G.Arnold, “Verilog Digital – Computer Design”, Prentice Hall (PTR), 1999.

Course Code	:	**EC5119**
Course Title	:	**RF circuits**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Describe the Noise models for passive components and noise theory.
CO2	Analyse the design of a high frequency amplifier.
CO3	Compare different LNA topologies and design techniques.
CO4	Distinguish between different types of mixers.
CO5	Evaluate the various types of synthesizers, oscillators and their characteristics.

Course Content:

Basic concepts in RF design - units in RF Design, time variance - Effects of Non-linearity, harmonic distortion, gain compression, cross modulation, intermodulation, cascaded nonlinear stages, AM/PM conversion Characteristics of passive IC components at RF frequencies – interconnects, resistors, capacitors, inductors and transformers – Transmission lines. Noise – classical two-port noise theory, noise models for active and passive components

High frequency amplifier design – zeros as bandwidth enhancers, shunt-series amplifier, f T doublers, neutralization and unilateralization

Low noise amplifier design – LNA topologies, power constrained noise optimization, linearity and large signal performance

Mixers – multiplier-based mixers, subsampling mixers, diode-ring mixers. Oscillators and synthesizers – describing functions, resonators, negative resistance oscillators, synthesis with static moduli, synthesis with dithering moduli, combination synthesizers – phase noise considerations.

RF power amplifiers – Class A, AB, B, C, D, E and F amplifiers, modulation of power amplifiers, linearity considerations

Text Books:

1. Thomas H. Lee, “The Design of CMOS Radio-Frequency Integrated Circuits”, 2nd ed., Cambridge, UK: Cambridge University Press, 2004.
2. B.Razavi, “RF Microelectronics”, 2nd Ed., Prentice Hall, 1998.

Reference Books:

1. Abidi, P.R. Gray, and R.G. Meyer, eds., “Integrated Circuits for Wireless Communications”, New York: IEEE Press, 1999.
2. R. Ludwig and P. Bretchko, “RF Circuit Design, Theory and Applications”, Pearson, 2000.

Course Code	:	**EC5120**
Course Title	:	**DSP Architecture**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Explain the architecture details of fixed and floating point DSPs.
CO2	Infer control instructions, interrupts, and pipeline operations, memory and buses.
CO3	Illustrate the features of on-chip peripheral devices and their interface.
CO4	Implement signal processing algorithms and applications in DSPs.
CO5	Describe the architecture of advanced DSPs.

Course Content:

Fixed-point DSP architectures. TMS320C54X, ADSP21XX, DSP56XX architecture details. Addressing modes. Control and repeat operations. Interrupts. Pipeline operation. Memory Map and Buses. TMS320C55X architecture and its comparison.

Floating-point DSP architectures. TMS320C67X, DSP96XX architectures. Cache architecture. Floating-point Data formats. On-chip peripherals. Memory Map and Buses.

On-chip peripherals and interfacing. Clock generator with PLL. Serial port. McBSP. Parallel port. DMA. EMIF. Serial interface- Audio codec. Sensors. A/D and D/A interfaces. Parallel interfaceRAM and FPGA. RF transceiver interface

DSP tools and applications. Implementation of Filters, DFT, QPSK Modem, Speech processing. Video processing, Video Encoding / Decoding. Biometrics. Machine Vision. High performance computing (HPC).

Digital Media Processors. Video processing sub systems. Multi-core DSPs. OMAP. CORTEX, SHARC, SIMD, MIMD Architectures.

Text Books:

1. B.Venkataramani and M.Bhaskar, "Digital Signal Processor, Architecture, Programming and Applications", 2nd edition, McGraw- Hill, 2010.
2. S.Srinivasan and Avtar Singh, "Digital Signal Processing, Implementations using DSP Microprocessors with Examples from TMS320C54X", Brooks/Cole, 2004.

Reference Books:

1. S.M.Kuo and Woon-SengS.Gan, "Digital Signal Processors: Architectures, Implementations, and Applications", Printice Hall, 2004.
2. N. Kehtarnavaz and M. Kerama, "DSP System Design using the TMS320C6000", Printice Hall, 2001.

Course Code	:	**EC5121**
Course Title	:	**Physics and Modeling of MOS Transistors**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Develop mathematical models for modern MOS devices.
CO2	Identify solution to overcome short channel issues.
CO3	Analyze current distribution in bipolar transistor.
CO4	Design various compact models appropriate for industry.
CO5	Evaluate the performance parameters of FinFET.

Course Content:

MOS Capacitor: Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation, CV characteristics of MOS, LFCV and HFCV, Non-idealities in MOS, oxide fixed charges, interfacial charges.

The MOS transistor: Small signal modelling for low frequency and High frequency, PaoSah and Brews models; Short channel effects in MOS transistors.

The bipolar transistor: Ebers-Moll model; charge control model; small-signal models for low and high frequency and switching characteristics

Compact Modeling: Compact model Level 1, Level 2, Level 3, UTB/FD SOI MOSFET.

FinFETs: I-V characteristics, device capacitances, parasitic effects of extension regions, performance of simple combinational gates and amplifiers, novel circuits using FinFETs and GAA devices.

Text Books:

1. S. M. Sze, "Physics of Semiconductor Devices" 2nd edition, Wiley Eastern, 1981.
2. M. Lundstrom, "Fundamentals of Nanotransistors", World Scientific Publishing Co Pte Ltd 2017.

Reference Books:

1. Y. P. Tsividis, "Operation and Modelling of the MOS Transistor", McGraw-Hill, 1987.
2. E. Takeda, "Hot-carrier Effects in MOS Transistors", Academic Press, 1995.

Course Code	:	**EC5122**
Course Title	:	**Nano-Scale Devices: Modelling and Circuits**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Describe the MOSFET devices and their mechanisms.
CO2	Explain the physics behind the operation of multi-gate systems.
CO3	Design circuits using nano-scaled MOS transistors.
CO4	Analyze the Radiation effects in SOI MOSFETs.
CO5	Evaluate the performance parameters of the digital and analog circuits.

Course Content:

MOSFET scaling, short channel effects - channel engineering - source/drain engineering - high k dielectric - copper interconnects - strain engineering, SOI MOSFET, multigate transistors – single gate – double gate – triple gate – surround gate, quantum effects – volume inversion – mobility – threshold voltage – inter subband scattering, multigate technology – mobility – gate stack

MOS Electrostatics – 1D – 2D MOS Electrostatics, MOSFET Current-Voltage Characteristics – CMOS Technology – Ultimate limits, double gate MOS system – gate voltage effect - semiconductor thickness effect – asymmetry effect – oxide thickness effect – electron tunnel current – two dimensional confinement, scattering – mobility

Silicon nanowire MOSFETs – Evaluvation of I-V characteristics – The I-V characteristics for nondegenerate carrier statistics – The I-V characteristics for degenerate carrier statistics – Carbon nanotube – Band structure of carbon nanotube – Band structure of graphene – Physical structure of nanotube – Band structure of nanotube – Carbon nanotube FETs – Carbon nanotube MOSFETs – Schottky barrier carbon nanotube FETs – Electronic conduction in molecules – General model for ballistic nano transistors – MOSFETs with 0D, 1D, and 2D channels – Molecular transistors – Single electron charging – Single electron transistors

Radiation effects in SOI MOSFETs, total ionizing dose effects – single-gate SOI – multi-gate devices, single event effect, scaling effects

Digital circuits – impact of device performance on digital circuits – leakage performance trade off – multi VT devices and circuits – SRAM design, analog circuit design – transconductance - intrinsic gain – flicker noise – self heating –band gap voltage reference – operational amplifier – comparator designs, mixed signal – successive approximation DAC, RF circuits.

Text Books:

1. J P Colinge, “FINFETs and other multi-gate transistors”, Springer – Series on integrated circuits and systems, 2008.

Reference Books:

1. Mark Lundstrom and Jing Guo, “Nanoscale Transistors: Device Physics, Modeling and Simulation”, Springer, 2006.

Course Code	:	**EC5123**
Course Title	:	**CMOS Digital VLSI**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Compare different CMOS circuits using various logic families and circuit layout.
CO2	Use tools for VLSI IC design.
CO3	Apply RC and linear delay models.
CO4	Design combinational circuits of CMOS logic families.
CO5	Devise sequential circuits such as latches and flip-flop.

Course Content:

Review of MOS cap and MOS transistor models, Non-ideal behavior of the MOS Transistor. Transistor, Short channel effects, velocity saturation. Inverter characteristics,

Noise margin analysis. Integrated Circuit Layout: Design Rules, Parasitics. Delay: RC Delay model, linear delay model, Elmore delay model, ON resistance and fall delay.

Interconnect and Robustness in CMOS circuit layout. Inverter transient response, dynamic power, short circuit power, leakage and transistor stacks.

Combinational Circuit Design: CMOS logic families including static, dynamic and dual rail logic. Gate sizing, logic gate capacitance, gate delay, parasitic delay, load capacitance delay, logical effort, buffer insertion, input ordering, and skewed gates. Other logic families-pseudo NMOS, domino logic, transmission gates.

Adders and multipliers. Introduction to pipelining. Sequential Circuit Design: Static circuits. Design of latches and Flip-flops. Latch delay constraints and latch timing analysis.

Text Books:

1. N.H.E. Weste and D.M. Harris, "CMOS VLSI design: A Circuits and Systems Perspective", 4th Edition, Pearson Education India, 2011.
2. L. Glaser and D. Dobberpuhl, "The Design and Analysis of VLSI Circuits", Addison Wesley, 1985.

Reference Books:

1. C. Mead and L. Conway, "Introduction to VLSI Systems", Addison Wesley, 1979.
2. J. Rabaey, "Digital Integrated Circuits: A Design Perspective", Prentice Hall India, 1997

Course Code	:	**EC5124**
Course Title	:	**Physical Design Automation**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Describe VLSI design automation tools.
CO2	Solve the performance issues in circuit layout.
CO3	Analyze physical design problems and employ appropriate automation algorithms.
CO4	Identify solution to large mapping problem.
CO5	Evaluate circuits using both analytical and CAD tools.

Course Content:

VLSI design automation tools- algorithms and system design. Structural and logic design. Transistor level design. Layout design. Verification methods. Design management tools

Layout compaction, placement and routing. Design rules, symbolic layout. Applications of compaction. Formulation methods. Algorithms for constrained graph compaction. Circuit representation. Wire length estimation. Placement algorithms. Partitioning algorithms

Floor planning and routing- floor planning concepts. Shape functions and floor planning sizing. Local routing. Area routing. Channel routing, global routing and its algorithms.

Simulation and logic synthesis- gatelevel andswitch level modeling and simulation. Introduction to combinational logic synthesis. ROBDD principles, implementation, construction and manipulation. Two level logic synthesis.

High-level synthesis- hardware model for high level synthesis. Internal representation of input algorithms. Allocation, assignment and scheduling. Scheduling algorithms. Aspects of assignment. High level transformations.

Text Books:

1. S.H. Gerez, “Algorithms for VLSI Design Automation”, JohnWiley (India), 2006.
2. N.A.Sherwani, “Algorithms for VLSI Physical Design Automation”, Kluwer, 2012.
3. S.M. Sait, and H. Youssef, “VLSI Physical Design Automation”, Cambridge India, 2010.

Reference Books:

1. M.Sarrafzadeh, “Introduction to VLSI Physical Design”, McGraw Hill (IE), 1996.
2. Giovanni De Micheli, “Synthesis and Optimization of Digital Circuits”, McGraw Hill, 2017.
3. Andrew B. Kahng and Jens Lienig, “VLSI Physical Design: From Graph Partitioning to Timing Closure”, Springer, 2011.

Course Code	:	**EC5125**
Course Title	:	**Asynchronous System Design**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Summarize the fundamentals of asynchronous protocols.
CO2	Analyse the performance of Asynchronous System and implement handshake circuits.
CO3	Describe the various control circuits and Asynchronous system modules.
CO4	Use high level languages and tools for Asynchronous Design.
CO5	Apply commands and control flow of Balsa language for implementing Asynchronous Designs.

Course Content:

Fundamentals: Handshake protocols, Muller C-element, Muller pipeline, Circuit implementation styles, theory. Static data-flow structures: Pipelines and rings, Building blocks, examples

Performance: A quantitative view of performance, quantifying performance, Dependency graphic analysis. Handshake circuit implementation: Fork, join, and merge, Functional blocks, mutual exclusion, arbitration and metastability.

Performance: A quantitative view of performance, quantifying performance, Dependency graphic analysis. Handshake circuit implementation: Fork, join, and merge, Functional blocks, mutual exclusion, arbitration and metastability.

High-level languages and tools: Concurrency and message passing in CSP, Tangram program examples, Tangram syntax-directed compilation, Martin's translation process, Using VHDL for Asynchronous Design. An Introduction to Balsa: Basic concepts, Tool set and design flow, Ancillary Balsa Tools

The Balsa language: Data types, Control flow and commands, Binary/Unary operators, Program structure. Building library Components: Parameterized descriptions, Recursive definitions. A simple DMA controller: Global Registers, Channel Registers, DMA control structure, The Balsa description.

Text Books:

1. Chris. J. Myers, "Asynchronous Circuit Design", John Wiley and Sons, 2001.
2. Kees Van Berkel, "Handshake Circuits An Asynchronous architecture for VLSI programming", Cambridge University Press, 2004.

Reference Books:

1. Jens Sparso and Steve Furber, Kluver, "Principles of Asynchronous Circuit Design", Academic Publishers, 2001.
2. Richard F. Tinder, "Asynchronous Sequential Machine Design and Analysis", 2009.

Course Code	:	**EC5126**
Course Title	:	**Testability of Analog / Mixed-Signal Circuits and High-Speed Circuit Design**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Describe the basic testing methods and parametric measurements.
CO2	Develop testing models for ADC .
CO3	Discuss the concepts of analog channel testing and DFT techniques.
CO4	Design high speed op-amps.
CO5	Apply the concepts of high speed data converters.

Course Content:

Overview of Mixed-signal Testing. DC and Parametric Measurements. DAC Testing: Basics of converter testing, Basic DC tests, Transfer curve tests, Dynamic DAC tests, DAC Architectures.

ADC Testing: ADC testing versus DAC testing, DC tests and Transfer curve tests, Dynamic ADC tests, ADC Architectures. Sampling Theory. DSP based testing: Advantages of DSP based testing, DSP, Discrete-time transforms, The Inverse FFT.

Analog Channel Testing. Fundamentals of RF Testing. Design for Test: Overview, Advantages of DFT, Digital Scan, Digital BIST, Digital DFT for Mixed-signal circuits, Mixed-signal boundary scan and BIST, Ad-hoc Mixed signal DFT, RF DFT.

High speed design techniques: High Speed Op-amps, High Speed op-amp applications, RF/IF Subsystems

High Speed sampling and High Speed ADCs, High Speed DACs and DDS systems.

Text Books:

1. Mark Burns, Gordon W. Roberts, “An Introduction to Mixed-signal IC test and Measurement”.
2. Walt Kester, “High Speed Design Technique”, Analog Devices, 1996.

Reference Books:

1. Linda S. Milor, “A Tutorial Introduction to Research on Analog and Mixed-Signal Circuit Testing”, IEEE Transactions on circuits and systems-II: Analog and Digital signal processing, Vol. 45, No. 10, October 1998.
2. Brian Lowe, “The Fundamentals of Mixed Signal Testing”.

Course Code	:	**EC5127**
Course Title	:	**VLSI Digital Signal Processing Systems**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Explain the concepts and algorithms of DSP.
CO2	Compute round off noise and numerical strength reduction.
CO3	Design Bit level arithmetic architectures.
CO4	Perform redundant arithmetic operation.
CO5	Analyze the effects of numerical strength reduction.

Course Content:

An overview of DSP concepts, Representations of DSP algorithms. Systolic Architecture Design: FIR Systolic Array, Matrix-Matrix Multiplication, 2D Systolic Array Design. Digital Lattice Filter Structures: Schur Algorithm, Derivation of One-Multiplier Lattice Filter, Normalised Lattice Filter, Pipelining of Lattice Filter

Scaling and Round off Noise - State variable description of digital filters, Scaling and Round off Noise computation, Round off Noise in Pipelined IIR Filters, Round off Noise Computation using state variable description, Slow-down, Retiming and Pipelining

Bit level arithmetic Architectures- parallel multipliers, interleaved floor-plan and bit-plane-based digital filters, Bit serial multipliers, Bit serial filter design and implementation, Canonic signed digit arithmetic, Distributed arithmetic

Redundant arithmetic -Redundant number representations, carry free radix-2 addition and subtraction, Hybrid radix-4 addition, Radix-2 hybrid redundant multiplication architectures, data format conversion, Redundant to Non-redundant converter.

Numerical Strength Reduction - Subexpression Elimination, Multiple Constant Multiplication, Subexpression Sharing in Digital Filters, Additive and Multiplicative Number Splitting.

Text Books:

1. K.K.Parhi, “VLSI Digital Signal Processing Systems”, John-Wiley, 2007.

Reference Books:

1. U. Meyer -Baese, “Digital Signal Processing with FPGAs”, Springer, 2014.

Course Code	:	**EC5128**
Course Title	:	**Internet of Things**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Identify the components of Internet of Things.
CO2	Choose wireless devices to build IoT applications.
CO3	Apply the functions of Raspberry Pi /Arduino/Equivalent platform in IoT applications.
CO4	Analyze the functions of sensors in IoT applications.
CO5	Develop IoT based applications.

Course Content:

Definition and Characteristics of IoT - Challenges and Issues - Physical Design of IoT, Logical Design of IoT - IoT Functional Blocks, Security.

Control Units – Communication modules – Bluetooth – Zigbee – Wifi – GPS- IOT Protocols (IPv6, 6LoWPAN, RPL, CoAP etc.), MQTT, Wired Communication, Power Sources

Four pillars of IOT paradigm, - RFID, Wireless Sensor Networks, SCADA (Supervisory Control and Data Acquisition), M2M - IOT Enabling Technologies - BigData Analytics, Cloud Computing, Embedded Systems.

Working principles of sensors – IOT deployment for Raspberry Pi /Arduino/Equivalent platform – Reading from Sensors, Communication: Connecting microcontroller with mobile devices – communication through Bluetooth, wifi and USB - ContikiOSCooja Simulator.

Clustering, Clustering for Scalability, Clustering Protocols for IOT

The Future Web of Things – Set up cloud environment –Cloud access from sensors– Data Analytics for IOT- Case studies- Open Source ‘e-Health sensor platform’ – ‘Be Close Elderly monitoring’ – Other recent projects.

Text Books:

1. Dieter Uckelmann et.al, “Architecting the Internet of Things”, Springer, 2011
2. Arshdeep Bahga and Vijay Madisetti, “Internet of Things – A Hand-on Approach”, Universities press, 2015.

Reference Books:

1. Charalampo Doukas, “Building Internet of Things with the Arduino”, Create space, April 2002.
2. Dr. OvidiuVermesan and Dr. Peter Friess, “Internet of Things: From research and innovation to market deployment”, River Publishers 2014.

Course Code	:	**EC5129**
Course Title	:	**Cognitive Radio**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Design filter banks using DFT and DWT approaches.
CO2	Develop application using CORIC.
CO3	Illustrate different demodulation schemes.
CO4	Discuss the rapid advances in Cognitive radio technologies.
CO5	Apply OFDM system model for cognitive radio.

Course Content:

Filter banks-uniform filter bank. Direct and DFT approaches. Introduction to ADSL Modem. Discrete multitone modulation and its realization using DFT. QMF. STFT. Computation of DWT using filter banks.

DDFS- ROM LUT approach. Spurious signals, jitter. Computation of special functions using CORDIC. Vector and rotation mode of CORDIC.CORDIC architectures.

Block diagram of a software radio. Digital down converters and demodulators Universal modulator and demodulator using CORDIC. Incoherent demodulation - digital approach for I and Q generation, special sampling schemes. CIC filters. Residue number system and high speed filters using RNS. Down conversion using discrete Hilbert transform. Under sampling receivers, Coherent demodulation schemes

Concept of Cognitive Radio, Benefits of Using SDR, Problems Faced by SDR, Cognitive Networks, Cognitive Radio Architecture. Cognitive Radio Design, Cognitive Engine Design.

A Basic OFDM System Model, OFDM based cognitive radio, Cognitive OFDM Systems, MIMO channel estimation, Multi-band OFDM, MIMO-OFDM synchronization and frequency offset estimation. Spectrum sensing to detect Specific Primary System, Spectrum Sensing for Cognitive OFDMA Systems

Text Books:

1. J. H. Reed, “Software Radio”, Pearson, 2002.
2. U. Meyer – Baese, “Digital Signal Processing with FPGAs”, Springer, 2004.
3. H. Arslan “Cognitive Radio, Software Defined Radio and Adaptive Wireless Systems”, University of South Florida, USA, Springer, 2007.
4. J. H. Reed, “Software Radio: A modern Approach to Radio Design”, Pearson, 2002

Reference Books:

1. S. K. Mitra, “Digital Signal processing”, McGrawHill, 1998.
2. K.C.Chen and R.Prasad, “Cognitive Radio Networks”, Wiley, 2009.
3. T. W. Rondeau, and C.W.Bostian, “Artificial Intelligence in Wireless Communications”, 2009.
4. Tusi, “Digital Techniques for Wideband receivers”, Artech House, 2001.

Course Code	:	**EC5130**
Course Title	:	**Reliability of Devices and Circuits**
Number of Credits	:	**3-0-0-3**
Prerequisites (Course code)	:	**None**
Course Type	:	**Elective**

Course outcomes: At the end of the course, the student will be able to:

CO1	Define the reliability of electronic devices and circuits.
CO2	Analyze the failure mechanisms of electronic devices and circuits.
CO3	Apply the concept of yield in electronic manufacturing.
CO4	Solve reliability issues in VLSI design.
CO5	Predict circuit performance using reliability models.

Course Content:

Background and Introduction: Definitions of reliability, failure modes, mechanisms, Basic concepts – Reliability functions, Relationship between these functions – Baths tubs curve – Exponential failure density and distribution functions - Expected value and standard deviation of Exponential distribution – Measures of reliability – MTTF, MTTR, MTBF

Introduction to mathematical methods for reliability: Failure rates, Normal distribution function, Six Sigma, Exponential, Weibull and Lognormal distributions for reliability modeling. Manufacturing yields.

Physics of failure based models for devices: Mass transport-induced failures (electromiration and stress voiding), Electronic charge-induced failures (Dielectric breakdown, Hot carrier effects, Electrical over-stress and Electrostatic discharge), Environmental damage (moisture ingress, corrosion, radiation damage), Degradation of interconnects (solder creep and fatigue).

Circuit Performance considering NBTI, PBTI, oxide breakdown, random telegraph noise, radiation damage, impact of parasitic effects, process temperature variation, Electromagentic compatibility (EMC), Electromagnetic Interference (EMI) and Electrostatic Discharge (ESD).

Introduction to semiconductor device packaging: Materials and processes used for semiconductor device packaging, stresses induced because of packaging.

Text Books:

1. M. Ohring, “Reliability and Failure of Electronic Materials and Devices”, First Edition, Academic Press, 1998.
2. J.W. McPherson, “Reliability Physics and Engineering”, Second Edition, Springer, 2013.

Reference Books:

1. Yuan Taur and T. Ning, “Fundamentals of Modern VLSI Devices”, Cambridge University Press, 1998.
2. J.Ross, “Microelectronic Failure Analysis”, Sixth Edition, ASTM International, 2011.