Dr.G.Seetharaman
Professor,
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Indian institute of Information Technology Tiruchirappalli.

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Education

- Ph.D – 2009- VLSI Design (ECE) –
  National Institute of Technology, Tiruchirappalli -620 015
- M.E. – 2002- Communication Systems
  Regional Engineering College, Tiruchirappalli -620 015
- B.E. (PT) – 1997 -Electronics and Communication Engineering
  Regional Engineering College, Tiruchirappalli – 620 015
- D.E.C.E - 1991 -Electronics and Communication Engineering
  State Board of Technical Education, Tamil Nadu

Experience

- Currently working as Professor in the Department of ECE,
  IIIT Tiruchirappalli
- Registrar (i/c), IIIT Tiruchirappalli, from 15.04.2021
- Officer on Special Duty – Auroville Foundation, (under MoE), Auroville - from 06.12.2021
- Secretary (additional charge)- Auroville Foundation, (under MoE), Auroville - 13.06.2018 to 21.09.2019
- Registrar (on deputation) - National Institute of Technology, Puducherry - 26.09.2018 to 15.11.2019
- Associate Professor IIIT Tiruchirappalli - 2019 – 2022
- Associate Professor - National Institute of Technology, Nagaland – 01.06.2016 to 02.12.2019
- Principal and Professor - Oxford Engineering College, Tiruchirappalli - 1.08.2008 to 30.05.2016

Key Position

- Point of contact – MoU signed between Indian Institute of Technology Madras (IITM), and Auroville Foundation, (under MoE), Auroville to establish a Learning Centre in Auroville and a Satellite Centre in IITM for promotion and development of new technologies for urban and rural housing, planning and architecture.
- Member of Board of Governors – IIIT Tiruchirappalli, from 26.10.2022 to till 2025.
- Member Secretary (Ex-officio)- Board of Governors, IIIT Tiruchirappalli, from 15.04.2021
- Member Secretary (Ex-officio)- Finance Committee, IIIT Tiruchirappalli, from 15.04.2021
- Member Secretary (Ex-officio)- Building and Works Committee, IIIT Tiruchirappalli, from 15.04.2021
- Member Secretary (Ex-officio)- Senate Committee, IIIT Tiruchirappalli, from 15.04.2021
- Member of Governing Board – Auroville Foundation, (under MoE), Auroville - from 2022
- Member of Finance Committee – Auroville Foundation, (under MoE), Auroville from 2022
- Member of Organisation and Goverence Committee - from 2022
- Secretary (Auroville Town Development Council) – Auroville Foundation, (under MoE), Auroville - from 2022
- Member Co-ordinator for the NATIONAL ASSESSMENT AND ACCREDITATION COUNCIL (NAAC) for conducting assessment and accreditation of Higher Educational Institutions (HEI) such as colleges, universities or other recognised institutions to derive an understanding of the 'Quality Status' of the institution.

Academic responsibilities

- Head of the Department, IIIT Tiruchirappalli, from 01.01.2020
- Admission (UG & PG)-Chairman, IIIT Tiruchirappalli, Since 2020
- Dean (Research & Consultancy), NIT Nagaland, 2017 - 2018
- TEQIP-III Co-ordinator, NIT Nagaland, 2017 - 2018

Administrative responsibilities

- Chief Vigilance Officer, IIIT Tiruchirappalli from 2021
- Chief Vigilance Officer, Auroville Foundation, from 2022
- Central Public Information Officer (CPIO), IIIT Tiruchirappalli & Auroville Foundation, from 2022
- Director's Advisory Committee, NIT Nagaland - 2018

Research Areas

- FPGA based system Design
- ASIC
- NoC
- Wireless transceivers
- Low Power VLSI Design
- VLSI based Signal Processing

List of Projects

- Chips to Startup (C2S) Programme-Special Manpower Development Program for Chips to System Design (SMDP-C2SD), Category-II: Development of Application Oriented Working Prototype of IPs/ASICs/SoCs- Ultra-low-power Shakti's RISC-V based Lightweight Edge AI Processor for IoT enabled healthcare applications- Chief Investigator Ministry of Electronics & Information Technology (MeitY), New Delhi-110003, 2024 – 2029 (5 years), Rs. 96/- Lakh.
- An Efficient optimization of large-scale data automation using VLSI based Artificial Intelligence/Machine Learning Algorithm- Principal Investigator - funded by Auroville Foundation, Auroville under Ministry of Education, New Delhi -2022-2024 – Rs. 8.4/- lakhs.
- Design and development of algorithms for integration of enterprise-wide data using AI techniques – Co- Principal Investigator - funded by Auroville Foundation, Auroville under Ministry of Education, New Delhi- -2022-2024 – Rs. 10.2/- lakhs.
- Principal Investigator and single point of contact for the value of Rs. 1737.5/- Crores (One Thousand Seven Hundred and Thirty-Seven Crore) for a period of three years (ongoing from 2022) to execute the projects related to Making of Auroville City.

- Novel approaches in the Design of Reliable Custom Topology for Application Specific Network-on-Chip – Principal Investigator - DST - UKIERI Thematic Partnership with university of Edinburg – (2015 – 2018) - Rs. 40/- lakhs.
- Installation of ASIC CAD Tools – Principal Investigator – funded by AICTE- (2009 – 2011) – Rs. 15/- Lakhs.

Other achievements

- Entrepreneurship Vision 2010" Entrepreneurship Development Programme - Principal Investigator – funded by AICTE- 2010 – 2013 – Rs. 6/- Lakhs.

Research Doctor of Philosophy (Ph.D)

Name of Candidate	Thesis Title	Year of award	Role
Bhargava. D. S IIIT Tiruchirappalli	Analysis of Beamforming Architectures for Multi-channel RF Transceivers	On-going	Supervisor
V.Kavitha IIIT Tiruchirappalli	A VLSI Architecture for Spectrum Sensing in Cognitive Radio and Optimization Technique for Spectrum Allocation	On-going	Supervisor
S. Vaishnavi IIIT Tiruchirappalli	Application of Nanotechnology in Energy Harvesting	On-going	Supervisor
B.Madusudhanan IIIT Tiruchirappalli	Block Chain Technology	On-going	Co-Supervisor
Jayshree National Institute of Technology Nagaland	Design of High Performance and Low Energy Consumption 2-D and 3-D Secured Reliable Network-on-Chip Interconnect for Application-Specific SoC	2022	Supervisor
N.Poornima OEC, Trichy	Design and Analysis of Different Topologies in Application Specific Network on Chip	2021	Co-Supervisor
A.Venkata Subramanian, JCET, Trichy	Algorithm & VLSI Architecture for Wavelet based Image Compression	2017	Supervisor

P.RengabPrabhu, OEC, Trichy.	Design and Analysis of Synchronous, Asynchronous & Wave-Pipelined Techs. for DSP Applications using ASIC	2015	Supervisor
M.Maheswari, JJCET, Trichy	Novel approaches in the Design of Reliable Custom Topology for Application Specific Network on Chip	2014	Supervisor

Post Graduate Dissertations Guided

Sl. No.	Name of Candidate	Title of Dissertation	Year of award
1.	Mr.Ateeque Ahmed Rizvi	Design of novel error correction coding with crosstalk avoidance for reliable on-chip interconnection link in Network On Chip(NOC)	2017
2.	Mr. Lakki Reddy Pavan Kumar Reddy	Partial reconfiguration on Network On Chip in Xilinx FPGA using custom topology	2017
3.	Mr.InukurthiJaswanth	Implementation of different multipliers on ZYNQ-7000 board	2017
4.	Mr.SeizalalSingson	Design of low power Network On Chip	2017
5.	Mr.P. Ezhilarasi	CORDIC Based Digital Down Converter for Software Defined Radio	2014
6.	Mr.N.Sivarajan	Design and Implementation of CORDIC for SDR	2014
7.	Mr.T. Nagasundaram	Design and Implementation of Asynchronous Circuits using Concurrent Reset	2013
8.	Ms.C. Suganya	Design of Portable Hearing AID based on FPGA	2012
9.	Ms.P. Sivakamasundari	Implementation of an Effective Algorithm for Network on Chip in FPGA	2011
10.	Ms.M. Ahilamary	Four-Bank Single-Port Memory Block for Symbol Reinter leaver Architecture	2010
11.	Ms.T. Daisy Rani	FPGA Implementation of Discrete Wavelet Transform using Flipping Structure	2010
12.	Mr.Virin	Built in Self-Test Based Design of Wave-Pipelined Circuits in ASICs	2008
13.	Mr.Venugopalchary	Synthesis Techniques for Implementation of Wave-Pipelined Circuits in ASICs	2008
14.	Mr. Sanjay G. Talekar	Implementation of time interleaved SAR ADC for UWB Application	2008

Under Graduate Dissertations Guided

Sl.No.	Name of Candidate	Title of Project	Year of award
1.	E Aakash, P Aditya Venkatesh and B Leelavardhan	Sparse signal recovery using Verilog and implementation on FPGA	2023
2.	Cherukuri Venkat Keshav Sai Auchitya Bussa S Sai Venkata Kishan Kumar	Real Time Face Alteration	2022
3.	B.Praveen N.T.S.S.Srinivas R.Harsha Vardhan	Automated Protection kit Which detects Face Mask And Temperature	2022
4.	Lavanya S	Low Dropout Regulators/ Analog Circuit Design	2022
5.	D. Arun Kumar M. Suhas Cristy Ravindra Jaiswar	Smart Irrigation System Using IoT	2021
6.	Jamisetti Vikas babu Doddi Bhanu prakash	Smart Health Monitoring System	2021
7.	Sesha Surya sai Satwik Reddy Bhuvanesh.S	Design of a 3-Port Router For Network On Chip (NoC)	2020
8.	Ankit Pal Choying Konyak Yabangkumla	Implementation of OFDM using FPGA	2017

Centre of Excellence

Sl.No.	Name of the Lab	Institute name
1.	INTEL VLSI LAB	Texas Instruments & National Institute of Technology, Nagaland
2.	ASIC CAD LAB	Oxford Engineering college, Tiruchirappalli

Journal Publications

1. Vaishnavi S, and Seetharaman G, "Device modelling and optimization of various n-i-p configurations for MASnI3 perovskite solar cells to achieve high efficiency using Solar Cell Capacitance Simulator-1D" Materials Today Communications, Elsevier, 37 (2023) 107007.
2. Poornima Narayanasamy, & Seetharaman Gopalakrishnan, "Novel Fault Tolerance Topology using Corvus Seek Algorithm for Application Specific NoC" Integration The VLSI journal, Elsevier, Volume 89, Pages 146-154, March 2023.
3. Kulandaivel Balakrishnan, Ramasamy Dhanalakshmi, and Gopalakrishnan Seetharaman, "S-shaped and V-shaped binary African vulture optimization algorithm for feature selection", Journal on Expert Systems, Wiley, 2022.
4. Jayshree, G. Seetharaman, and Debadatta Pati, "Design and Area Performance Energy Consumption Comparison of Secured Network-on-Chip with PTP and Bus Interconnections", J. Inst. Eng. India Ser. B 103, Springer, pp.1479–1491 2022.
5. Jayshree, G. Seetharaman, and Debadatta Pati, "Energy Consumption and Performance Comparison of DE Optimization and PSO based IP Core Mapping Techniquefor 2-D and 3-D Network-on-Chip" Semiconductor Science and Technology, 2021.
6. Jayshree, G. Seetharaman, and Debadatta Pati, "Enhanced TACIT Encryption and Decryption Algorithm for Secured Data Routing in 3-D Network-on-Chip based Interconnection of SoC for IoT Application" Journal of Scientific and Industrial Research, 2021.
7. Jayshree, G. Seetharaman, and Debadatta Pati, "Reliable Fault-tolerance Routing Technique for Network on chip Interconnect", Lecture Notes in Networks and Systems" Springer-2021.
8. Jayshree, G. Seetharaman, and Debadatta Pati, "Latency and Power Consumption Comparison at Different Technology Node of Hybrid Optimizations Technique for On-chip Interconnect in Multimedia SoCs" Advances in Parallel Computing, IOS Press-2021.

9. Poornima Narayanasamy, Santhi Muthurathinam & Seetharaman Gopalakrishnan, “Custom NoC Topology Generation using Discrete Antlion Trapping Mechanism”, The VLSI journal Integration, Elsvier, vol. 76, 2021.
10. Poornima Narayanasamy, Santhi Muthurathinam & Seetharaman Gopalakrishnan, “Design of Crosstalk Prevention Coding scheme based on Quintuplicated Manchester error correction method for Reliable on chip Interconnects” Advances in Electrical and Computer Engineering, vol. 18, no. 4, 2021.
11. Poornima Narayanasamy, Santhi Muthurathinam & Seetharaman Gopalakrishnan, “Dolphin Echolocation Based Generation of Application Definite Noc Custom Topology” International Journal of Recent Technology and Engineering (IJRTE), Volume-8 Issue-3, September 2019.
12. Godwin Enemali, Adewale Adetomi, G. Seetharaman & Tughrul Arslan, “A functionality-based runtime relocation system for circuits on heterogeneous FPGAS” IEEE, Transactions on Circuits and Systems II, Volume: 65, Issue: 5, May 2018.
13. Maheswari. M, and Seetharaman. G, “Enhanced Low Complex Double Error Correction Coding w ith Crosstalk Av oidance for Reliable On- Chip Interconnection Link” International journal Electron Test, DOI 10.1007/s10836-014-5465-5, Springer,. July 2014.
14. Seetharaman. G, “ASIC implementation of Multiplier free modified flipping architecture for Image compression” International journal of Advanced Science Letters, Volume 20, Numbers 10-12, pp. 2055-2059(5), October 2014.
15. Rengaprabhu. P, Venkatasubramanian. A, and Seetharaman. G, “FPGA and ASIC implementation of CORDIC using wave-pipelining” International journal of Advanced Science Letters, Volume 20, Numbers 10-12, pp. 2234-2238(5), October 2014.
16. Seetharaman. G, “FPGA implementation of Multiplier free architecture for Image compression” International journal of Advanced Science Letters, Volume 20, Numbers 10-12, pp. 2050-2054(5), October 2014.

17. Venkatasubramanian. A, Rengaprabhu. P, and Seetharaman. G, “Implementation of one level and two level 2D DWT using ASIC” International journal of Advanced Science Letters, Volume 20, Numbers 10-12, pp. 2239-2243(5), October 2014.
18. Maheswari. M, and Seetharaman. G, “Multi Bit Random and Burst Error Correction Code with Crosstalk Avoidance for Reliable On Chip Interconnection Links" International journal of Microprocessors and Microsystems, 37 (2013), pp. 420–429, Elsevier, March 2013.
19. Maheswari. M, and Seetharaman. G, “Design of novel error correction coding with cross talk aviodence for reliable On Chip Interconnects Links” International journal computer applications in technology, Inder science enterprises limited. 2013
20. Prabakar.T.N, Lakshminarayanan.G, and Seetharaman. G, “Design and Implementation of SoPC based Low Power Asynchronous Image Processor” Applied Mechanics and Materials Vols. 239-240 (2013) pp 1179-1183© (2013) Trans Tech Publications, Switzerland.
21. Maheswari. M, and Seetharaman. G, “Hamming Product Code Based Multiple Bit Error Correction Coding Scheme Using Keyboard Scan Based Decoding for On Chip Interconnects Links” Applied Mechanics and Materials Vols. 241-244 (2013) pp 2457-2461© (2013) Trans Tech Publications, Switzerland.
22. G. Seetharaman and B. Venkataramani, “Automation Schemes for FPGA Implementation of Wave-Pipelined Circuits,” ACM, Trans. on Reconfigurable Technology and Systems, vol. 2, no. 2, article 11, 2009.
23. G. Seetharaman, B. Venkataramani and G. Lakshminarayanan, “VLSI implementation of Hybrid wave-pipelined 2D DWT using lifting Scheme”, Hindawi Publishing Corporation, Journal on VLSI, Article ID 512746, pp. 1-8, 2008.
24. G. Seetharaman, B. Venkataramani and G. Lakshminarayanan, “Automation techniques for implementation of Hybrid wave-pipelined 2D DWT”, Springer, Journal on Real-Time Image Processing, DOI 10.1007/s11554-008-0087-8, Springer-Verlag, 2008.

25. G. Seetharaman, B. Venkataramani and G. Lakshminarayanan, “Design and FPGA implementation of self-tuned wave-pipelined filters with Distributed Arithmetic Algorithm”, Springer, Research journal on circuits, systems and signal processing, 27: 261–276, 2008.
26. V. Amudha, B. Venkataramani and G. Seetharaman, “Design and system on chip implementation of image encoders”, WSEAS transactions on Circuits & systems, no. 10, vol. 4, pp 1292-1299, October 2005.
27. G. Seetharaman, B. Venkataramani and G. Lakshminarayanan, “Design and FPGA implementation of wave-pipelined lifting scheme for two level 2D-DWT ”, WSEAS transactions on Circuits & systems, no. 10, vol. 4, pp 1284-1291, October 2005.

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28. G. Seetharaman, B. Venkataramani and G. Lakshminarayanan, “Design and FPGA implementation self-tuned wave-pipelined filters,” IETE journal of research, vol 52, no.4, July-August 2006, pp. 305-313.

Conference papers:

29. Jayshree, G. Seetharaman, and Debadatta Pati, “Design of High-Performance HMRPD Net-work on Chip Interconnect for Neuromorphic Architectures”, 3rd International Conference on Energy, Power, and Environment (ICEPE 2020) National Institute of Technology Meghalaya, India. 5th - 7th March 2021.
30. Jayshree, G. Seetharaman, and Debadatta Pati, “R3ToS based Partially Reconfigurable Data Flow Pipelined Network on chip”, NASA/ESA Conference on Adaptive Hardware and Systems (AHS 2018), The University of Edinburgh, UK. August 6 - 9, 2018
31. Jayshree, G. Seetharaman, and Debadatta Pati, “Design and Analysis of Novel Interconnects with Network-On-Chip LVDS Transmitter for Low Delay”, NASA/ESA Conference on Adaptive Hardware and Systems (AHS 2018), The University of Edinburgh, UK. August 6 - 9, 2018.
32. Jayshree, G. Seetharaman, “Application Definite Fault Resistant Topology for IoT Networks” International Conference on Advanced computing & Communication Technologies (ICACCE -2018), ECE Paris, June 22 -23, 2018.

33. Poornima.N, G. Seetharaman, and Arslan Tughrul, “Design of Reconfigurable and Reliable Application Specific Network on Chip for R3TOS” The NASA/ESA Conference on Adaptive Hardware and Systems (AHS 2017) Caltech at Pasadena, CA, USA, July 24 - 27, 2017.
34. R,Ganesan, G.Seetharaman, T. Arslan, T.N.Prabakar, C.Vennila, “Design and Testing of Low Power Reliable NoCs for Wireless Applications” International Conference on Advanced computing & Communication Technologies, Panipat, Nov. 27-29, 2015.
35. Adewale Adetomi, Godwin Enemali, Ali Ebrahim, Tughrul Arslan, Xabier Iturbe, “R4thos –Based Mitigation of Power Analysis Attacks Using the XADC in Xilinx FPGAs” International Conference on Emerging Security Technologies (EST-2015), Technishe Unversity at Braurschweig, Germany, September 3-5, 2015.
36. Seetharaman. G, “ASIC implementation of Multiplier free modified flipping architecture for Image compression” in the International Conference on Internet Services Technology and Information Engineering (ISTIE 2014), at Bali, Indonesia, 31st May – 1st June 2014.
37. Rengaprabhu. P, Venkatasubramanian. A, and Seetharaman. G , “FPGA and ASIC implementation of CORDIC using wave-pipelining” in the International Conference on Internet Services Technology and Information Engineering (ISTIE 2014), at Bali, Indonesia, 31st May – 1st June 2014.
38. Seetharaman. G, “FPGA implementation of Multiplier free architecture for Image compression” International Conference on Internet Services Technology and Information Engineering (ISTIE 2014), at Bali, Indonesia, 31st May – 1st June 2014.
39. Venkatasubramanian. A, Rengaprabhu. P, and Seetharaman. G , “Implementation of one level and two level 2D DWT using ASIC” in ISTIE 2014, at Bali, Indonesia, 31st May – 1st June 2014.
40. Poornima. N, and Seetharaman. G, “FPGA Implementation of Less area overhead Radix – 4 Threshold Viterbi Decoder with trace forwarding for OFDM based Cognitive Radio,” IEEE-International Conference on Emerging Trends and Applications in Computer Science – 2013 (ICETACS - 2013) Sep.13 and 14 -2013, Department of Computer Science, St. Anthony's College, Shillong, Meghalaya.

41. Seetharaman. G, “A Novel Approach for an Efficient Implementation of 2 Level 2D Dwt Using ASIC & FPGA,” IEEE-International Conference on Emerging Trends and Applications in Computer Science – 2013, (ICETACS - 2013) Sep.13 and 14 -2013, Department of Computer Science, St. Anthony's College, Shillong, Meghalaya.
42. Venkatasubramanian. A, Rengaprabhu. P, and Seetharaman. G , “ASIC Implementation of One Level 2D-DWT Using Wave-Pipelining" IEEE- Asia Modeling Symposium 2013, (AMS2013) Hong Kong, 23 July 2013.
43. and Seetharaman. G, “Implementation of One Level 2D DWT Using Multiplier Less Modified Flipping Architecture" IEEE- Asia Modeling Symposium 2013, (AMS2013) Hong Kong, 23 July 2013.
44. Maheswari. M, and Seetharaman. G, “Implementation of Application Specific NOC Architectures on Reconfigurable device using Topology Generation Algorithm with Genetic Algorithm based optimization technique”. In the sixth International Conference on Information Processing, (ICIP-2012) at Bangalore, India, 10-12 August 2012.
45. Venkatasubramanian. A, Seetharaman. G, Prabakar. T.N. and Sheeba, “A Modified Algorithm for Removal of Salt and Pepper Noise in Color Images” in the 3rd IEEE International Conference on Intelligent Systems, Modelling and Simulation, ISMS2012, at Kota Kinabalu, Sabah, Malaysia, 8 – 10 February 2012.
46. Kavitha. A, Seetharaman. G, and Srinithi, “Design of Low Power TPG Using LP-LFSR” in the 3rd IEEE International Conference on Intelligent Systems, Modelling and Simulation, ISMS2012, at Kota Kinabalu, Sabah, Malaysia, 8 – 10 February 2012.
47. Rengaprabhu. P, Venkatasubramanian. A, and Seetharaman. G , “Design and Implementation of Automated Wave-Pipelined Circuit Using ASIC” in the 3rd IEEE International Conference on Intelligent Systems, Modelling and Simulation, ISMS2012, at Kota Kinabalu, Sabah, Malaysia, 8 – 10 February 2012.
48. Seetharaman. G, “A Novel Architecture for an Efficient Implementation of Image Compression Using 2D-DWT” in the 3rd IEEE International Conference on Intelligent Systems, Modelling and Simulation, ISMS2012, at Kota Kinabalu, Sabah, Malaysia, 8 – 10 February 2012.

49. Venkatasubramanian. A, Rengaprabhu. P, and Seetharaman. G , "Implementation of Hybrid Wave-pipelined 2D DWT Using ASIC" in the 3rd IEEE International Conference on Intelligent Systems, Modelling and Simulation, ISMS2012, at Kota Kinabalu, Sabah, Malaysia, 8 – 10 February 2012..
50. Venkatasubramanian. A, Rengaprabhu. P, and Seetharaman. G, "System on Chip implementation of wave-pipelined 2D DWT" in the WORLDCOMP-2011, International conference on Embedded system applications at Las Vegas, Nevada, July 18-21, 2011, USA.
51. Maheswari. M, and Seetharaman. G, "Design and Implementation of Low Complexity Router for Network on Chip using FPGA" in the WORLDCOMP-2011, International conference on Embedded system applications at Las Vegas, Nevada, July 18-21, 2011, USA.
52. Rengaprabhu. P, Venkatasubramanian. A, Parasuraman. S, Marimuthu. M, and Seetharaman. G, "Design and Implementation of SOC and BIST based Wave-Pipelined Circuit" in the WORLDCOMP-2011, International conference on Embedded system applications at Las vegas, Nevada, July 18-21, 2011, USA.
53. Dr. G.Seetharaman, M.Santhi, Roshan Silwal, & G.Lakshminarayanan "A Novel Online Clock Skew Scheme for FPGA Based Asynchronous wavepipelined Circuits" in the 5th International conference on Future Information Technology at Busan, May 21st – 23rd 2010,Korea.
54. V. Vireen, G. Seetharaman, and B. Venkataramani, "Built in Self Test Based Design of Wave-Pipelined Circuits in ASICs" Proceedings of IEEE International conference on VLSI Design 2008, Delhi, 5-9 January 2009.
55. N. Venugopalachary, V. Vireen, G. Seetharaman, and B. Venkataramani, "ASIC Implementation of Self Tuned Wave-Pipelined Circuits" Proceedings of IEEE International conference on Electronic Design 2008, Penang, Malaysia,1-3 December 2008.
56. V. Vireen, G. Seetharaman, and B. Venkataramani, "Synthesis Techniques for Implementation of Wave-Pipelined Circuits in ASICs" Proceedings of IEEE International conference on Electronic Design 2008, Penang, Malaysia,1-3 December 2008.

57. G. Seetharaman, and B. Venkataramani, "SOC implementation of wave-pipelined circuits," Proceedings of IEEE International conference on Field Programmable Technology 2007, pp. 9-16, Dec. 12-14, Japan.
58. V. Amudha , B. Venkataramani and G. Seetharaman, "Optimization techniques for the system on chip implementation of JPEG encoder," Proc. of the 5th WSEAS Int. Conf. on Signal Processing, Computational Geometry & Artificial Vision, , pp 94-101, September 15-17, 2005, Malta.
59. G. Seetharaman, B. Venkataramani and G. Lakshminarayanan, "Design and FPGA implementation of lifting scheme for 2D-DWT using wave-pipelining," Proc. of the 5th WSEAS Int. Conf. on Signal Processing, Computational Geometry & Artificial Vision, pp 53-60, September 15-17, 2005, Malta.
60. G. Seetharaman, B. Venkataramani, V. Amudha and Anurag Saundattikar, "System on chip implementation of 2D DWT using lifting scheme," Proc. of the International Asia and South Pacific Conference on Embedded SOCs (ASPICES 2005), July 5-8, 2005, Bangalore.

Published in National conference proceedings

61. N. Poornima and G. Seetharaman and "Design and implementation of Router on FPGA for NoC applications" Conference 8th May 2010, Anna University, Coimbatore.
62. G. Seetharaman, B. Venkataramani and G. Lakshminarayanan, "Design and FPGA implementation of wave-pipelined image block encoders using 2D-DWT," Proc. of VLSI design and test symposium VDAT 2005, pp. 12-20, Aug 2005, Bangalore.
63. G. Seetharaman, B. Venkataramani and G. Lakshminarayanan, "Design and FPGA implementation of wave-pipelined distributed arithmetic based filters," Proceedings of VLSI Design & Test workshop VDAT 2004, pp. 216-220, August 2004, Mysore.

Books/Monographs/Book chapters Publications

64. Jayshree, G. Seetharaman, and Debadatta Pati, "Reliable Fault-tolerance Routing Technique for Network on chip Interconnect", Lecture notes in Networks and Systems-Intelligent Sustainable Systems Springer-2021.
65. Jayshree, G. Seetharaman, and Debadatta Pati, "Comparative Study of Hybrid Optimizations Technique for On-Chip Interconnect in Multimedia SoCs", Smart Intelligent Computing and Communication Technology Advances in Parallel Computing, 2021.
66. Maheswari. M, and Seetharaman. G, "Implementation of Application Specific Network-On-Chip Architectures on Reconfigurable Device Using Topology Generation Algorithm with Genetic Algorithm Based Optimization Technique", R. Venugopal and L.M. Patnaik (Eds.): ICIP 2012, CCIS 292, pp. 436–445, 2012. Springer-Verlag Berlin Heidelberg 2012
67. G. Seetharaman, B.Venkataramani and G.Lakshminarayanan, "Design and FPGA implementation of wave-pipelined distributed arithmetic based filters", Progress in VLSI design and test 2004, Elite Publishing House (P) Ltd., New Delhi, 2005.

68. G. Seetharaman, B.Venkataramani and G.Lakshminarayanan, "Design and FPGA implementation of wave-pipelined image block encoders using 2D-DWT", Progress in VLSI design and test 2004, Elite Publishing House (P) Ltd., New Delhi, 2005.
69. Maheswari.M and Seetharaman. G, "Implementation of ASNOC Architectures on Reconfigurable device using Topology with Genetic Algorithm based optimization technique", Springer-Verlag Berlin Heidelberg 2012.
70. Dr.G.Seetharaman and Dr.G.Dhanalakshmi, "Emerging Trends in Engineering, Technology & Management", SELP Publication, Tamilnadu, 2015.

Seminars/Conferences/Short Term Courses/Summer Schools/Winter Schools Organized as Coordinator or Convener

S. No.	From	To	Title of the Program	Sponsoring Agency
1.	18.07.2022	24.07.2022	Science and Engineering Research Board (SERB) Sponsored High-End Workshop (Kaaryashala) on "IoT and Machine learning for Automation"	SERB
2.	31.01.2022	04.02.2022	Advanced Industrial Automation Training for Engineering Education and Research	IIITT & INDWELL Automation, Mangalore.
3.	22.11.2021	26.11.2021	AICTE Training and Learning (ATAL) Academy Sponsored Online Faculty Development Programme on "System on Chip design and testing:	AICTE
4.	01.03.2021	05.03.2021	A Five-Day Hands-on Workshop on NI Graphical System Design Platform for Engineering Education and Research	IIITT
5.	23.11.2020	27.11.2020	AICTE Training and Learning (ATAL) Academy Sponsored Online Faculty Development Programme on 'Design Challenges in VLSI and Embedded system for IoT Applications'	AICTE
6.	14.12.2020	18.12.2020	AICTE Training and Learning (ATAL) Academy Sponsored Online Faculty Development Program on 'Challenges and Opportunities in Data Science - A Research Perspective'	AICTE
7.	15.08.2018	19.8.2018	TEQIP III sponsored -STTP on Recent Advancement in Signal Processing	NIT Nagaland
8.	26.04.2018	30.04.2018	TEQIP III sponsored -Recent Trends in Nano Electronics	NIT Nagaland
9.	30.01.2018	03.02.2018	TEQIP III sponsored -workshop on Attaining the goal by enhancing the employability skills	NIT Nagaland
10.	14.05.2017	19.05.2017	TEQIP III sponsored - workshop on FPGA based VLSI Design training program using Intel FPGA software tools and development boards	NIT Nagaland

11.	21.05.2017	25.05.2017	TEQIP III sponsored -Induction Programme on University Human Values based on Co-Existential Philosophy	NIT Nagaland
12.	8.12.2014	15.12.2014	Faculty Development Training Programme on Embedded & Real Time Systems	ANNA University, Chennai
13.	16.06.2014	23.06.2014	Computer Architecture -Faculty Development Training Programme	ANNA University, Chennai
14.	16.12.2013	23.12.2013	VLSI Design- Faculty Development Training Programme	ANNA University, Chennai
15.	18.02.2013	22.02.2013	Entrepreneurship Awareness Programme	AICTE
16.	23.02.2012	25.02.2012	Workshop on "Network on Chip Architecture"	CSIR
17.	11.07.2011	13.07.2011	"Entrepreneurship Vision 2010" – Entrepreneurship Awareness Programme	AICTE
18.	27.08.2010	28.08.2010	SEMINR on "Software Defined Radio"	AICTE
19.	21.08.2010	21.08.2010	Research Methodologies	IETE
20.	12.11.2010	13.11.2010	Workshop on VLSI Applications in Higher data rate communications and Signal processing	DRDO
21.	27.08.2009	9.08.2009	"System on Chip" CONFERENCE	AICTE
22.	24.06.2009	03.07.2009	"Design, Testing & Formal Verification Techniques for Integrated circuits & systems" Staff Development Programme	AICTE

National or International conference organized as Chairman or Secretary

Sl. No.	Post held	Details of conference organized	Duration	
			From	To
1.	Chairman	CONFERENCE on "System on Chip"	27.08.2009	9.08.2009
2.	Secretary	Emerging trends in engineering and Management	06.04.2013	06.04.2013

Participation in International/National Conferences & Country Visited

Sl.No.	Country	Purpose of visit	Chair person
1	UNITED KINGDOM, SCOTLAND	University of Edinburgh	Project Discussion
2	INDONESIA	Presented paper in the Conference-ISTIE 2014	Received Best Paper Award
3	HONGKONG	Presented paper in the Conference-AMS 2013	Act as a Chair person for the session
4	MALAYSIA	Presented paper in the Conference-ISMS 2012 & ICED 2011	Act as a Chair person for the session
5	USA	Presented paper in the Conference-worldcomp11	
6	JAPAN	Presented paper in the Conference-ICFPT 2007	
7	SINGAPORE	Presented paper in the Conference	
8	Shillong, Meghalaya	IEEE-Presented paper in the International Conference- in Emerging trends and applications in computer science-ICETACS-2013-Review four papers for this conference	
9	Bangalore	South Zone co-ordinator for the CoreEL Digilent Design Contest-2013	

Fellowship/Membership of Professional Bodies

Sl. No.	Name of Professional Body	Grade of Membership	Membership No.
1.	ISTE	LIFE-Member	LM60210
2.	IETE	Associate	M210578
3.	CSI	Member	N1063535
4.	IEEE	Member	90564777